



# Scaling Up: SiC Epitaxy for Industrial Production

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# Outline

- **Introduction**
  - WBG materials for high power switching applications
  - SiC & onsemi
- **SiC epitaxy basics**
  - SiC properties
  - SiC epitaxy basic principles, parameters and structure
  - SiC epi defects
- **Technology for mass production**
  - Epi Reactors
  - Mass production process flow
  - Metrology
- **Evolution & challenges in SiC epitaxy**
  - Process control
  - Metrology - Epi thickness, defects control and classification

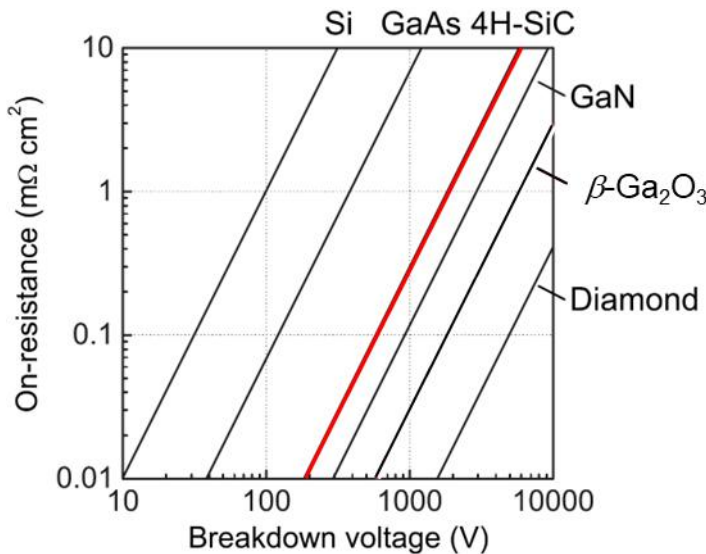
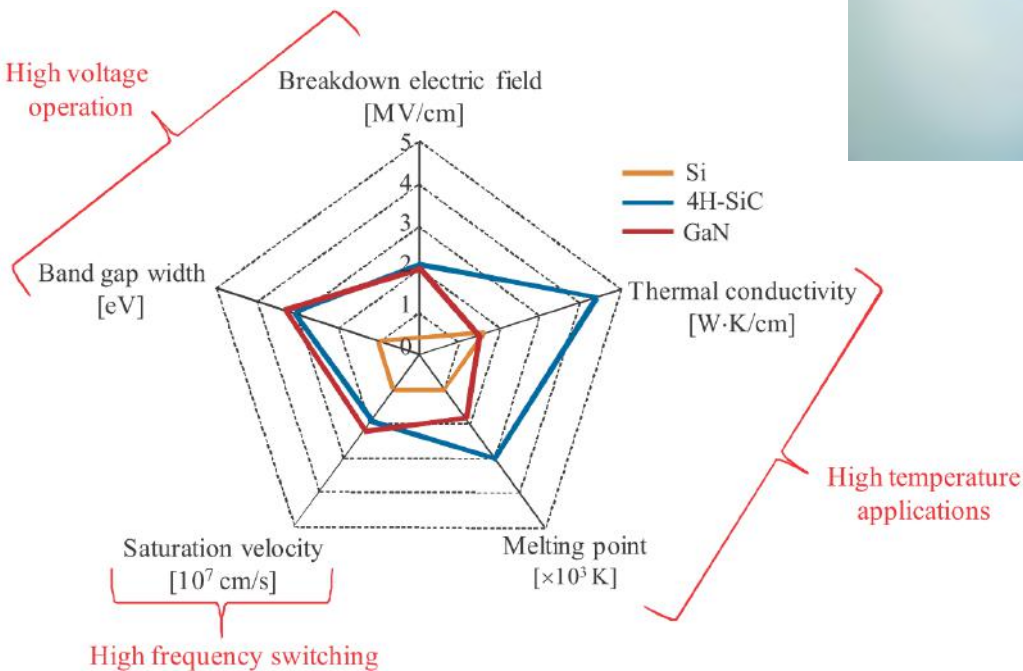


# Introduction



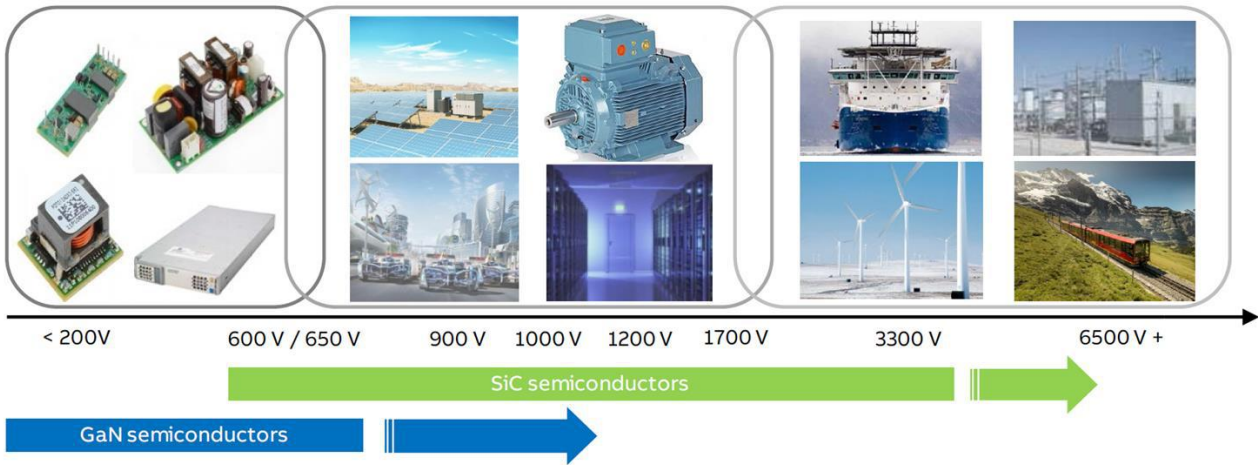
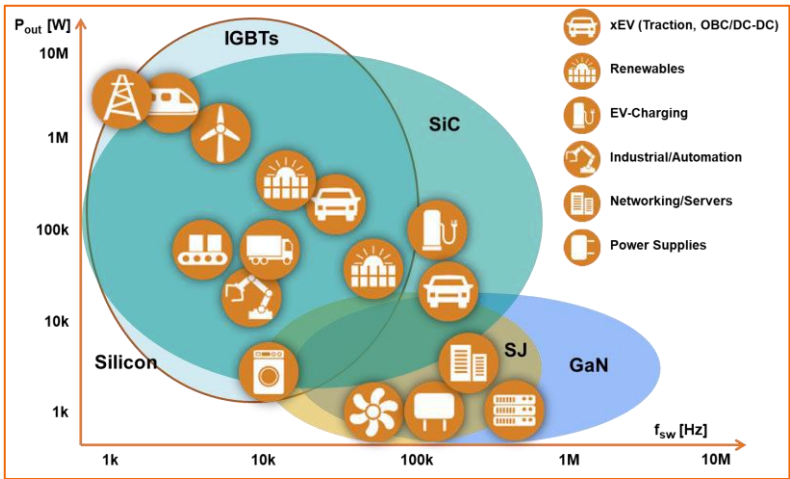
# Why wideband gap semiconducting materials?

WBG power devices offer lower resistance at high voltages, operation at high frequencies, and elevated temperature with reduced cooling

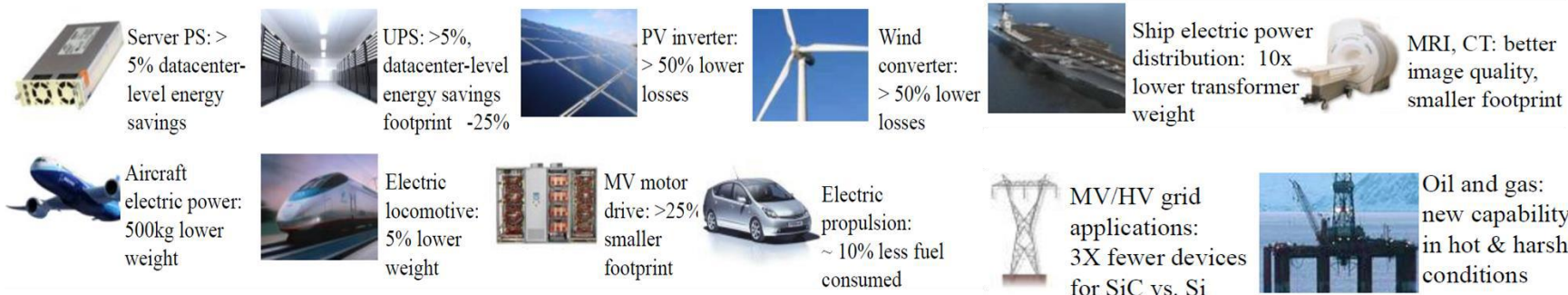


Theoretical limit of on-resistance as a function of breakdown voltage

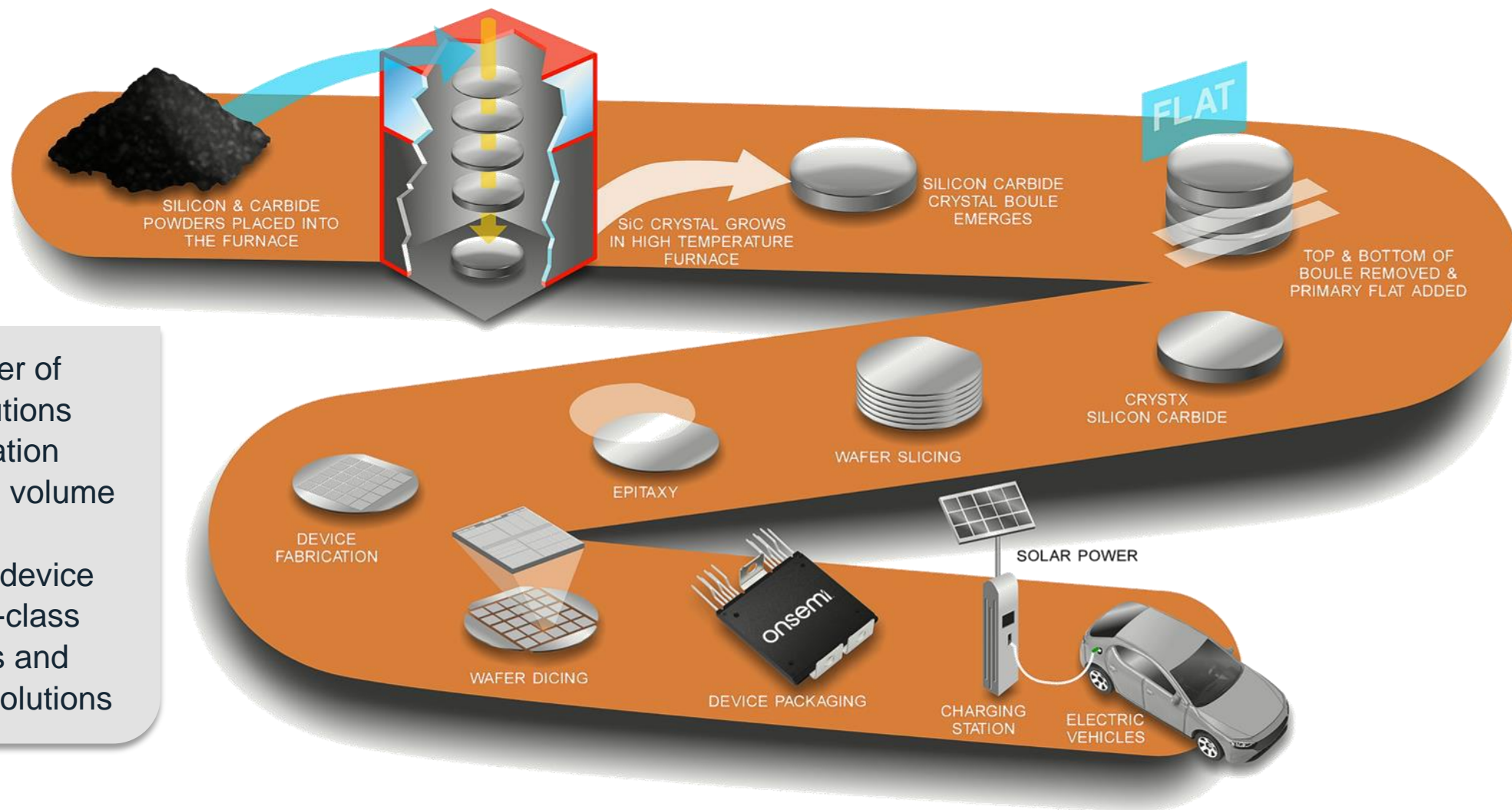
# Potential wideband gap converter applications



**SiC** and other WBG power devices offer lower resistance at high voltages, smaller footprint, operation at high frequencies, and elevated temperature with reduced cooling.



# onsemi Silicon Carbide Vertically Integrated Manufacturing



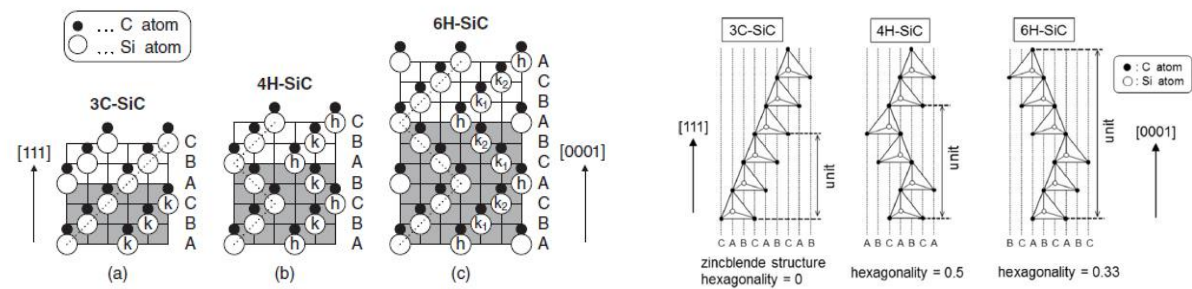
**onsemi** is a supplier of silicon carbide solutions with vertical integration capability including volume SiC boule growth, substrate, epitaxy, device fabrication, best-in-class integrated modules and discrete package solutions





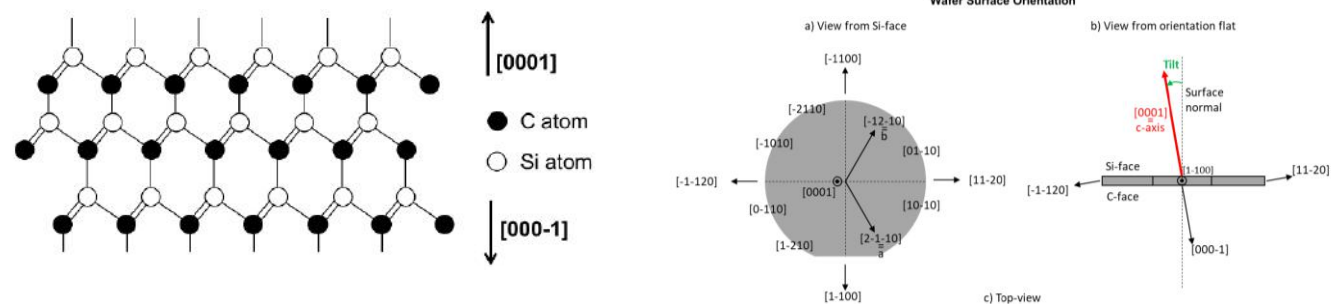
# SiC Epitaxy

# SiC crystal structure



Material	3C-SiC	6H-SiC	4H-SiC	Si
Bandgap (eV)	2.36	3.02	3.26	1.12
eMobility (cm <sup>2</sup> V <sup>-1</sup> s <sup>-1</sup> )	1000	100	1200	1400
E <sub>B</sub> (MeV cm <sup>-1</sup> )	1.4	3.0	2.8	0.3
BFOM (ε <sub>s</sub> μE <sub>B</sub> <sup>3</sup> ) Norm. to Si	61	63	626	1

- SiC crystal structure has different poly-types; cubic or hexagonal with different stacking sequences
- The polytype used for device fabrication today is 4H-SiC with a bandgap of 3.2 eV
  - 4H-SiC has the widest bandgap and best established material growth technology



- Carbon face & Silicon face: [0001] and [000-1] orientations are not equivalent
  - Different surface and material properties
- Si-face is the „front side“ (substrate polishing, epitaxial growth and device fabrication)
  - Si-face has a lower surface energy – smoother surface (but slower epi growth rates), less defects
  - C-face is mechanically harder – more difficult to polish; it is also more chemically reactive

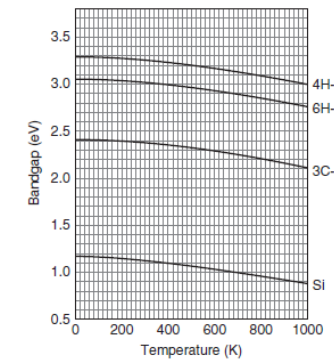
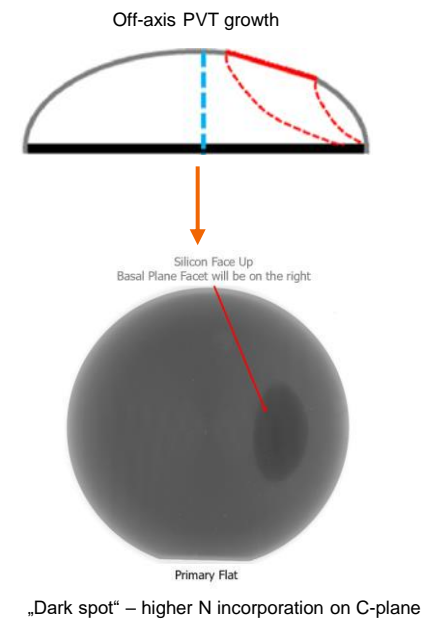


Figure 2.11 Temperature dependence of bandgap for several SiC polytypes.

Fundamentals of Silicon Carbide Technology. T. Kimoto, J. A. Cooper, 2014

T. Kimoto: Bulk and epitaxial growth of silicon carbide. Progress in Crystal Growth and Characterization of Materials 62 (2016) 329–351



# SiC epitaxy

- Epi growth on off-axis substrate is needed for homoepitaxial SiC polytype replication (miscut 4° towards  $\bar{1}\bar{1}20$ )

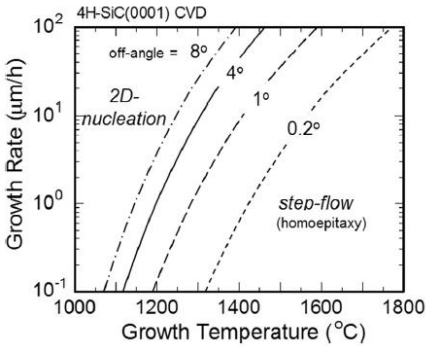
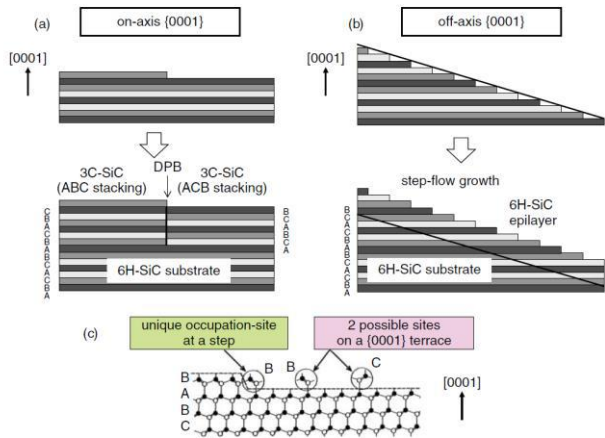


Figure 4.2 Schematic illustration of growth modes and stacking sequences of SiC layers grown on (a) on-axis 6H-SiC(0001) and (b) off-axis 6H-SiC(0001). (c) Bond configuration near an atomic step and on the (0001) terrace.

- Temperature: 1580 °C – 1650°C
- Pressure: 5-30 kPa
- Total flow (mostly H<sub>2</sub>): ~10<sup>2</sup> slm
- Growth rates: 5 – 70 μm/hour
- N-type doping with nitrogen

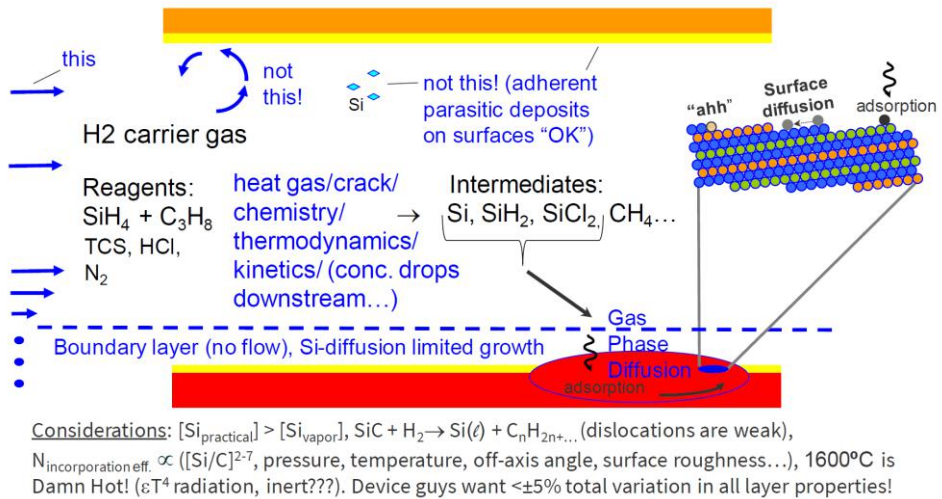
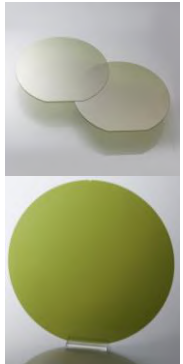
Function	Process gas
C-precursor (~10 <sup>2</sup> sccm)	C <sub>2</sub> H <sub>4</sub> , C <sub>3</sub> H <sub>8</sub>
Si-precursor (~10 <sup>2</sup> sccm)	SiH <sub>4</sub> , HCl <sub>3</sub> Si (TCS)
Carrier gas	H <sub>2</sub>
Dopant gas (~10 <sup>1-2</sup> sccm)	N <sub>2</sub> , NH <sub>3</sub>
Reduction of Si gas phase condensation	HCl

## 150mm (6inch) substrates

- 350 μm thick
- Orientation flat
- Well established worldwide supply chain, high quality

## 200mm (8inch) substrates

- 350-500 μm thick (reduction of warp from internal stress)
- Orientation notch
- Immature, expensive, but quick progress



Considerations:  $[Si]_{practical} > [Si]_{vapor}$ ,  $SiC + H_2 \rightarrow Si(l) + C_nH_{2n+...}$  (dislocations are weak),  $N_{incorporation} \propto ([Si/C]^{2-7}, \text{ pressure, temperature, off-axis angle, surface roughness...})$ , 1600°C is Damn Hot! ( $\epsilon T^4$  radiation, inert??). Device guys want  $< \pm 5\%$  total variation in all layer properties!

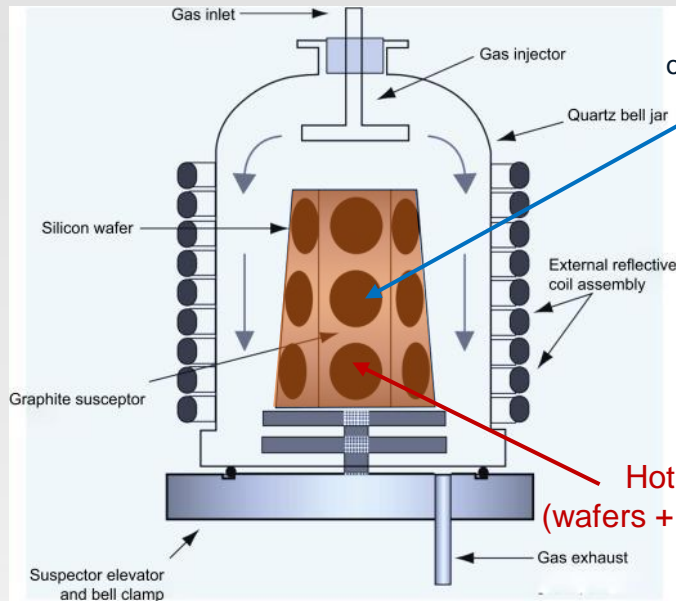
Epitaxial Materials Technology, PowerAmerica Short Course, Wolfspeed, 2020

T. Kimoto: Bulk and epitaxial growth of silicon carbide. Progress in Crystal Growth and Characterization of Materials 62 (2016) 329–351

Recent advances in 4H-SiC epitaxy for high-voltage power devices. Hidekazu Tsuchida, Materials Science in Semiconductor Processing Vol 78, May 2018, pp 2-12

# Si & SiC epitaxy: different worlds

## Silicon Epitaxy



Gases are decomposed only when they reach wafer surface and Si deposits immediately on wafer surface

Hot area  
(wafers + susceptor)

- Substrates are defect-free
- Only the susceptor and wafers are hot (usually by RF heating), the rest of the chamber is cold (below the gas decomposition temperature).  $[T] = 1000-1200^{\circ}\text{C}$ .
- Process gases are decomposed only at close proximity of the wafer and are immediately deposited on wafer.
- The process chamber thus remains clean and the epi growth process is time stable and predictable (autodoping & background doping).

## SiC epitaxy („hot-wall“)

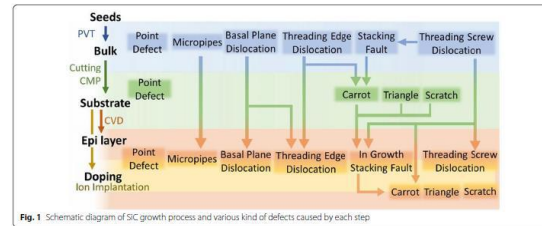


Fig. 1 Schematic diagram of SiC growth process and various kind of defects caused by each step

Gases are decomposed and react within the entire chamber volume and deposit at all surfaces

Deposits on injectors



Deposits on hood



Deposits on rotation & shields



- Substrates contain many defects
- The process gases are decomposed and react within the entire volume of the process chamber.  $[T] > 1600^{\circ}\text{C}$ !
- $\text{Si}_x\text{C}_y$  deposits accumulate at all surfaces of the process chamber, interacting and impacting the subsequent SiC deposition process.
- **Consequently, the SiC epitaxial process drifts and has to be constantly controlled via closed feedback loop using real time metrology data from just grown wafers.**
- Wafer, Epi cost > Process cost

# Growth rate

- Depending on reactor, main epi layer growth rate is 20–70 μm/hour
- Growth rate can be increased by:
  - Higher partial pressure of source gases – limited by Si clustering in gas phase
    - Can be suppressed by HCl, or system pressure decrease
  - Thinner boundary layer
    - Horizontal reactors (LPE, Aixtron, TEL): Increased total flow – has its limitation (H<sub>2</sub> consumption, pumping speed, epi uniformity)
    - Vertical reactors (NuFlare): Increase rotation speed, increased system pressure to some extent (via change of gas density; limited by Si clustering).

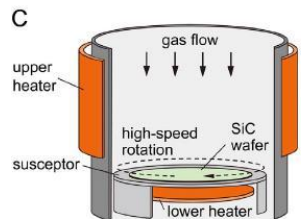
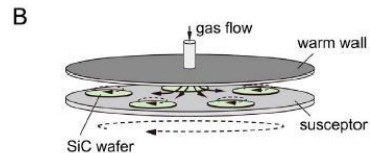
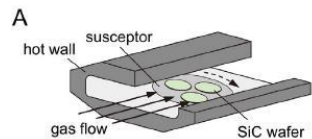
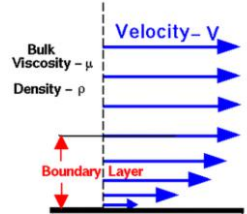


Fig. 1. Schematic illustration of (A) horizontal hot-wall, (B) planetary warm-wall and (C) vertical 4H-SiC epitaxial reactors.

Recent advances in 4H-SiC epitaxy for high-voltage power devices. Hidekazu Tsuchida, Materials Science in Semiconductor Processing Vol 78, May 2018, pp 2-12

$$Gr \propto \frac{p_x - p_e}{RT} \frac{D}{\delta}$$

$$\delta \propto \sqrt{\frac{\mu}{U\rho}}$$



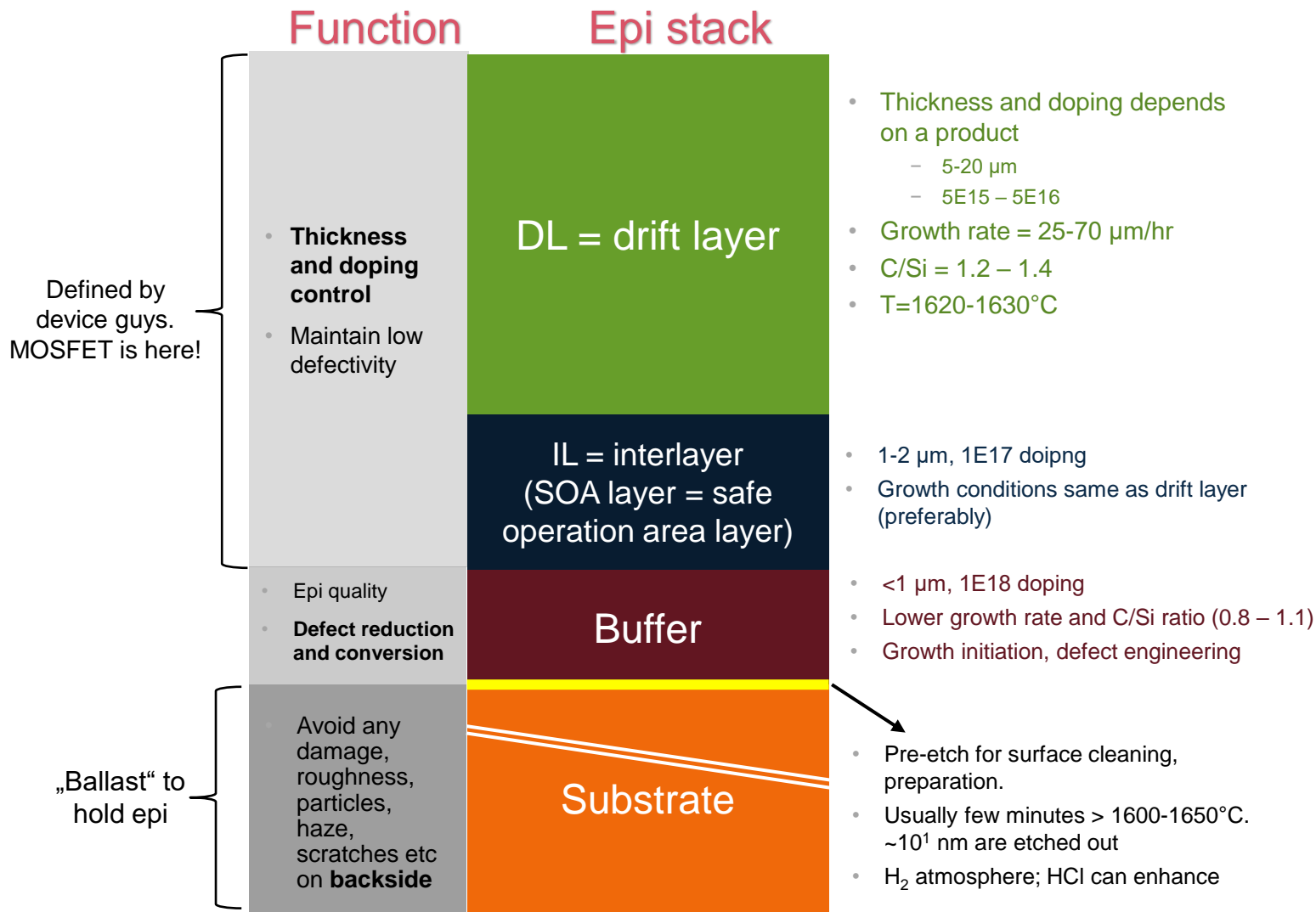
where  $p_x$  is the partial pressure of source gases outside the stagnant boundary layer,  $p_e$  is the equilibrium vapor pressure above the wafer surface,  $R$  is the gas constant,  $T$  is the growth temperature,  $D$  is the diffusion coefficient of the gas species,  $\delta$  is the thickness of the stagnant boundary layer,  $U$  is the gas-flow velocity,  $\mu$  is the viscosity and  $\rho$  is the gas density [50]. Under the fixed  $T$ , system pressure and input carrier gas-flow rate, where  $p_e$ ,  $D$ ,  $\rho$ ,  $U$  and  $\mu$  are assumed to be constant,  $Gr$  is expected to increase linearly with the input partial pressure of source gasses. When the Si partial pressure becomes higher, however, Si clusters can be formed by homogeneous nucleation in the gas phase as illustrated in Fig. 2 and limit enhancing growth rates.

$$\delta \propto \sqrt{\frac{\mu}{\omega\rho}}$$

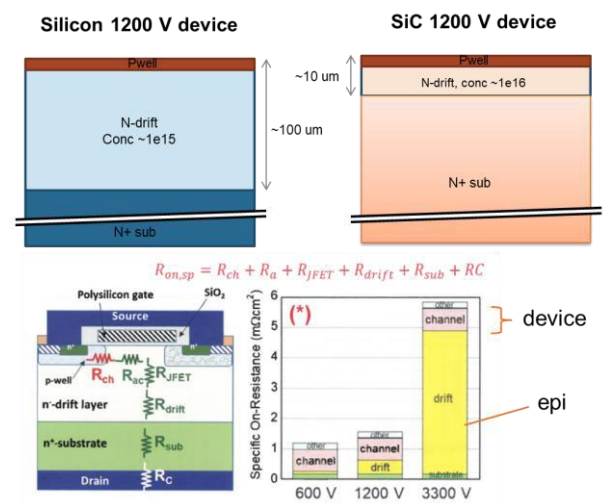
where  $\omega$  is the rotation speed [50,54,55] and applying high-speed wafer rotation can realize a thinning boundary layer and enhance growth rates under constant input H<sub>2</sub> carrier and source gas-flow rates.



# Typical SiC epitaxial layer stack (planar MOSFET)

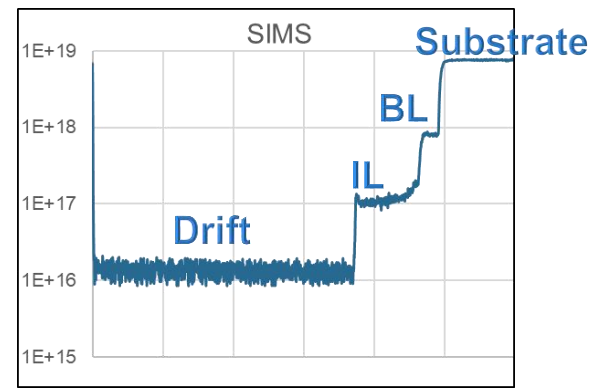


- Higher critical intensity of electric field – thinner drift region required for the same voltage rating



(\*\*) Figure from: J.W. Palmour, D.J. Lichtenwalner et al., IEEE Proc. ISPSD 2014, 79-82

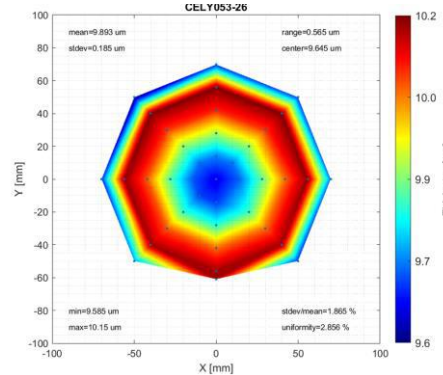
SIMS depth profile of nitrogen (dopant) in a typical SiC MOSFET epi stack



# SiC epitaxy process parameters

## Thickness control

- Precursor flow + growth time → target thickness
- $H_2$  carrier gas flow: depletion profile → thickness uniformity
- C/Si: Everything! ...Growth rate, thickness profile
- Temperature: Avoid large on-wafer variability.



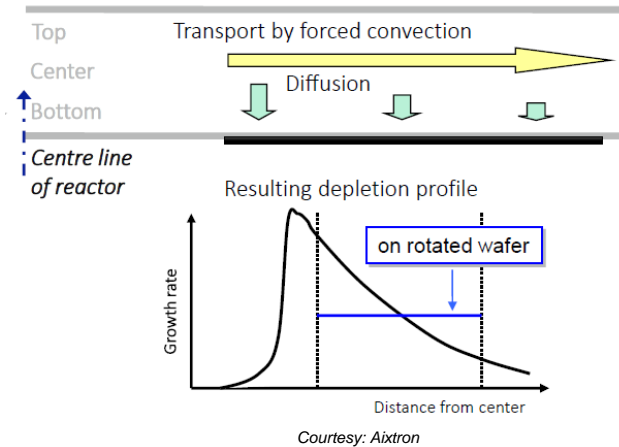
### Effect on thickness and doping profile

- C/Si ratio
- Carrier gas ( $H_2$ ) total flow and individual injector flows
- Temperature

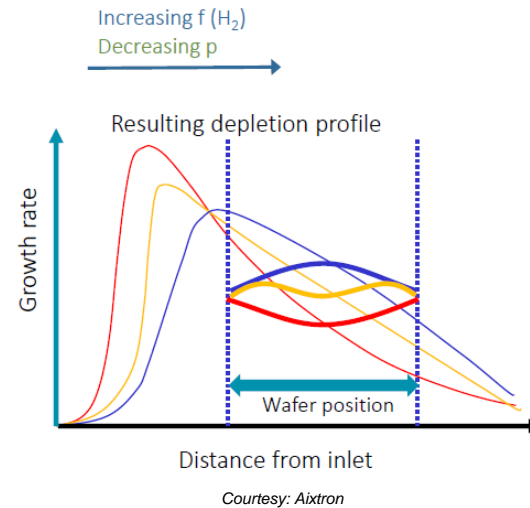
### Effect on surface quality and defects

- C/Si ratio
- Temperature
- Growth rate, precursors flow rates

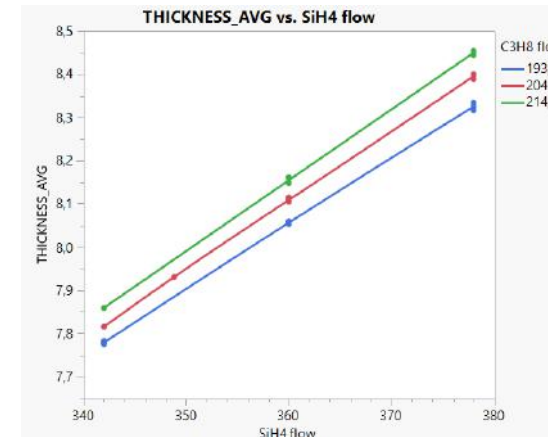
### Depletion profile in horizontal epi reactor



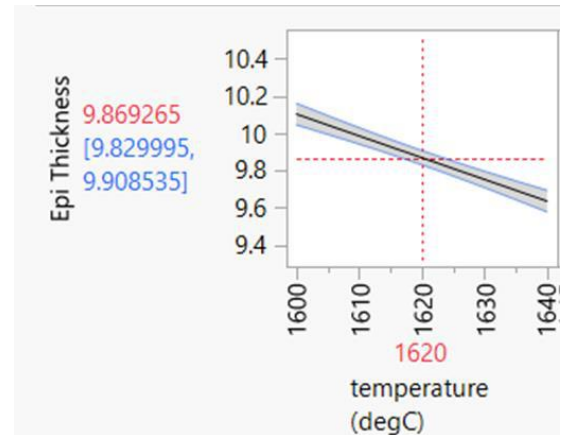
### Thickness uniformity fine tuning



Si-precursor flow rate determine growth rate. C-precursor flow rate influence is minor in usual C/Si ratio range.



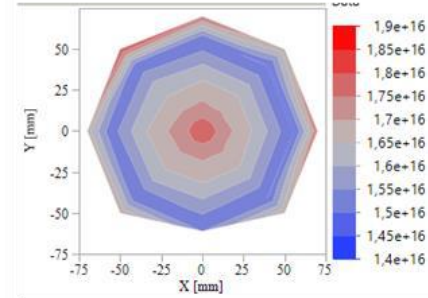
Temperature: Both direct and indirect influence. Vary between reactors.



# SiC epitaxy process parameters

## Doping control

- Dopant flow → target doping concentration
- C/Si: huge sensitivity due to C-N site competition
  - Also influence on doping profile
- Temperature: Minor influence, mainly through change of thickness.
  - Some reactors have intentionally center-edge T difference to compensate for other parameters center-edge variations



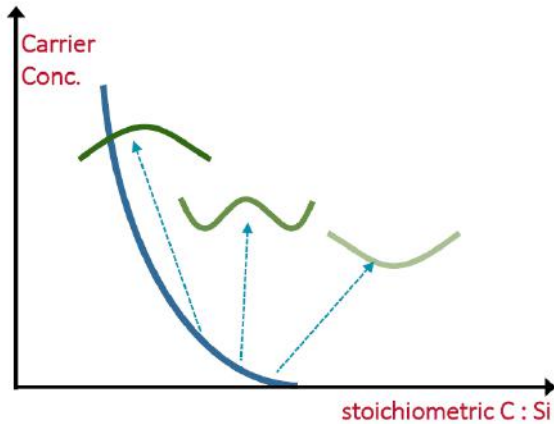
### Effect on thickness and doping profile

- C/Si ratio
- Carrier gas ( $H_2$ ) total flow and individual injector flows
- Temperature

### Effect on surface quality and defects

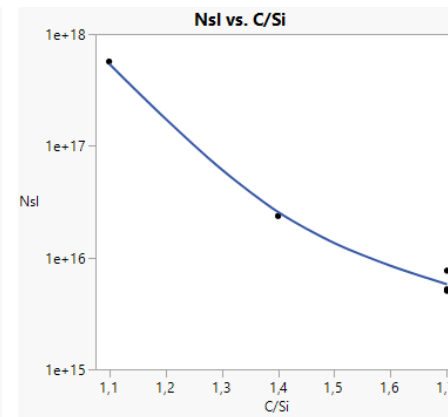
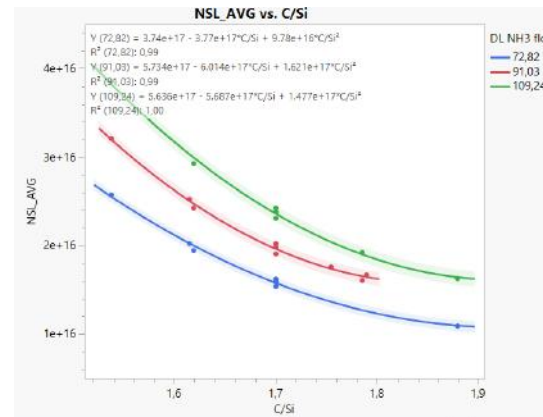
- C/Si ratio
- Temperature
- Growth rate, precursors flow rates

### Typical trend in horizontal epi reactors

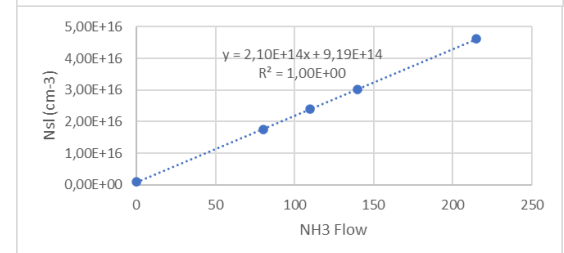
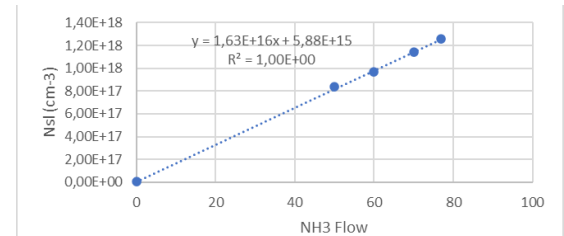


Courtesy: Aixtron

### Doping concentration sensitivity on C/Si ratio

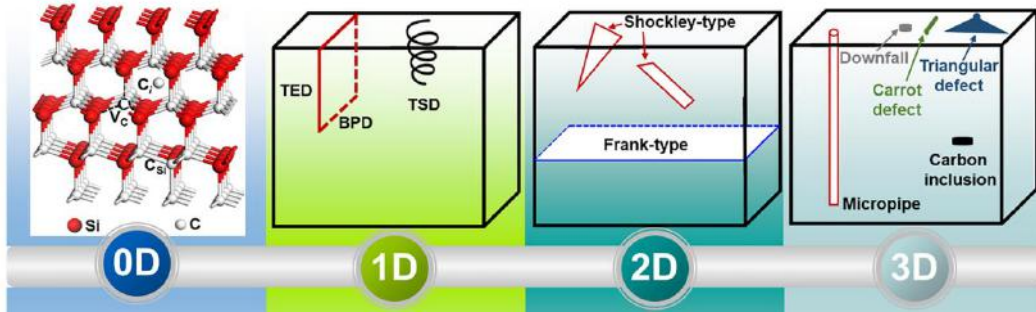


### Doping concentration vs. dopant flow: good linearity

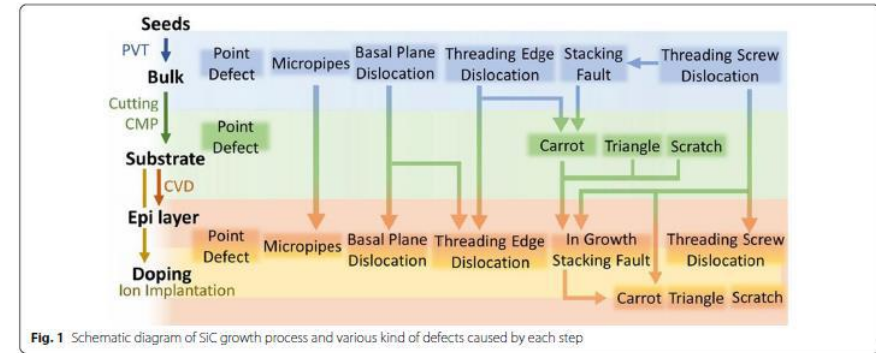




# Epi process & defects



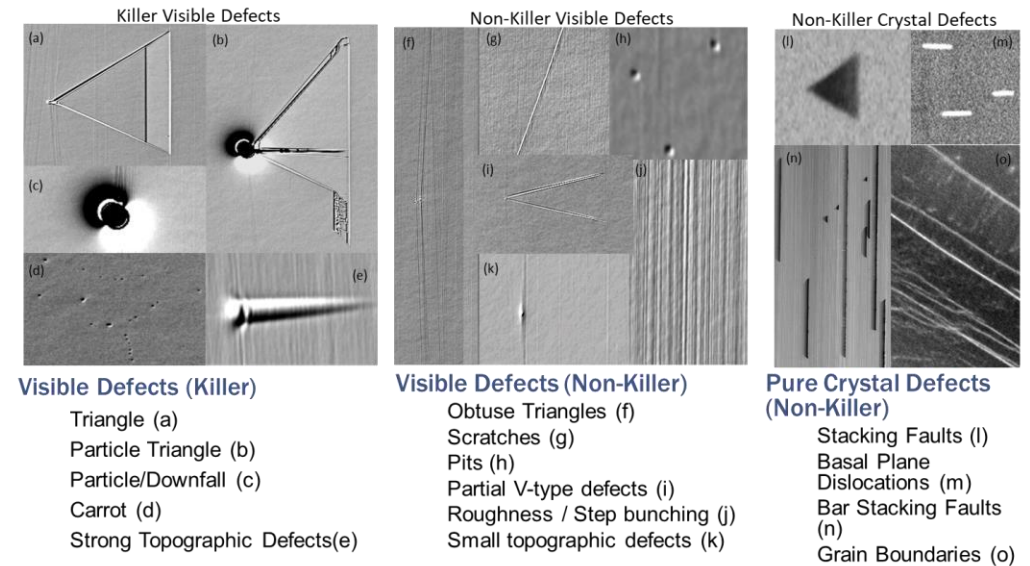
R. wang et al. Impurities and defects in 4H silicon carbide. Appl. Phys. Lett. 122, 180501 (2023)



Chen et al. Nanoscale Research Letters (2022) 17:30

- Extended Defect types in Epitaxial layers are well known and documented.
- Epi process:
  - Avoid generation of killer defects (Triangular) and non-killer defects (Stacking Faults)
  - Convert harmful defects to less harmful (BPD → TED)

	Dislocations	Burgers vector	Dislocation-line direction	Density (cm <sup>-2</sup> )
TDs	Micropipe (MP)	$nc$ ( $n = 3-10$ )	[0001]	<0.1
	Threading screw dislocation (TSD)	$c$	[0001]	$10^2-10^3$
	Threading mixed dislocation (TMD)	$c + a$	[0001]	
	Threading edge dislocation (TED)	$([11\bar{2}0]/3)a$	[0001]	$10^3-10^4$
BPDs	Integrated basal plane dislocation (BPD)	$([11\bar{2}0]/3)a$	In (0001) plane (predominantly along $[11\bar{2}0]$ )	$10^2-10^4$
	Decomposed BPD	$([10\bar{1}0]/3)a + ([01\bar{1}0]/3)a$	In (0001) plane	

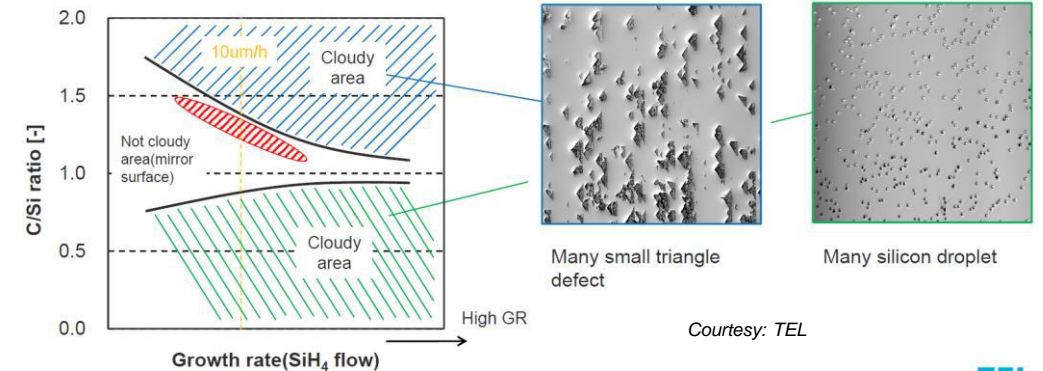


H. Das et al. Statistical Analysis of Killer and Non-Killer Defects in SiC and the Impacts to Device Performance. Materials Science Forum Vol. 1004, pp 458-463

# Epi process & defects

- Structural defects

- Stacking Faults – can nucleate from BPDs, TSDs in epi layer
  - Don't have surface feature, only PL signal
  - Partials (partial dislocations): border of 2D defects, usually SF. Can be visible.
  - Many types.
- Triangular defects, Carrot defects
- Carbon inclusions, polytype inclusions (PVT)
- Downfalls, particles
- Scratches



Stacking faults can expand upon electrical stress, increase on-resistance and leakage current

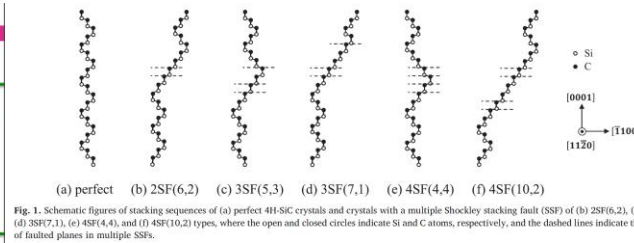
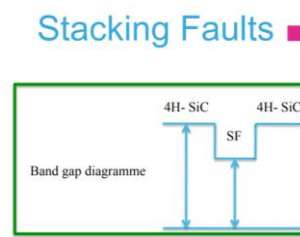
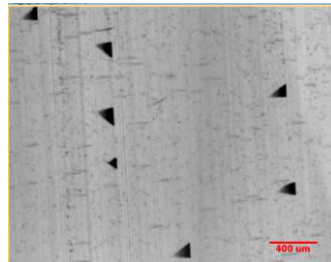
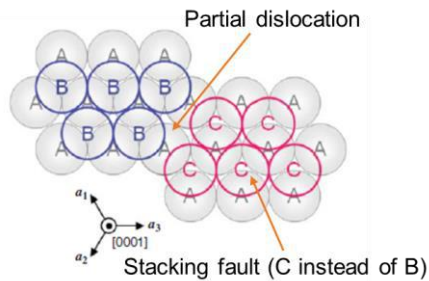


Fig. 1. Schematic figures of stacking sequences of (a) perfect 4H-SiC crystals and crystals with a multiple Shockley stacking fault (SSF) of (b) 2SF(6,2), (c) 3SF(5,3), (d) 3SF(7,1), (e) 4SF(4,4), and (f) 4SF(10,2) types, where the open and closed circles indicate Si and C atoms, respectively, and the dashed lines indicate the positions of faulted planes in multiple SSFs.

BPD split → SF

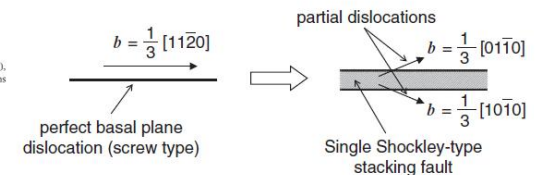


Figure 4.27 Schematic illustration of BPD split. A perfect BPD in SiC is dissociated into two partial dislocations, and a single Shockley-type stacking fault is created between the two partials.

Fundamentals of Silicon Carbide Technology. T. Kimoto, J. A. Cooper, 2014

# Epi process & defects

## Triangular defects – „killer“ defects

- Failure rate of a chip containing killer defect is close to 100%

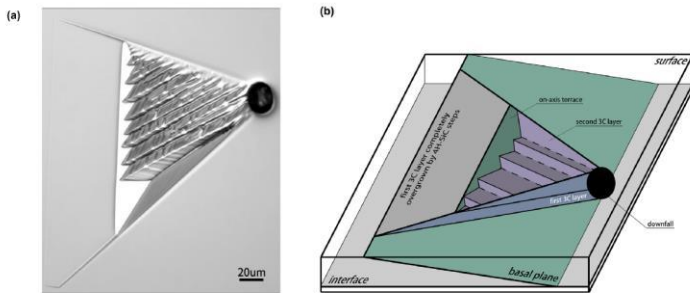
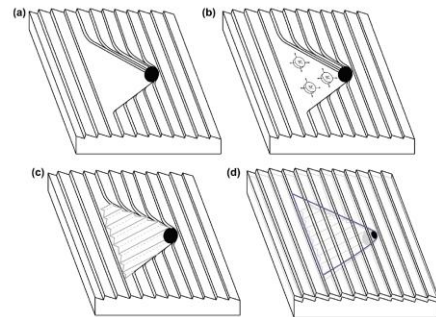
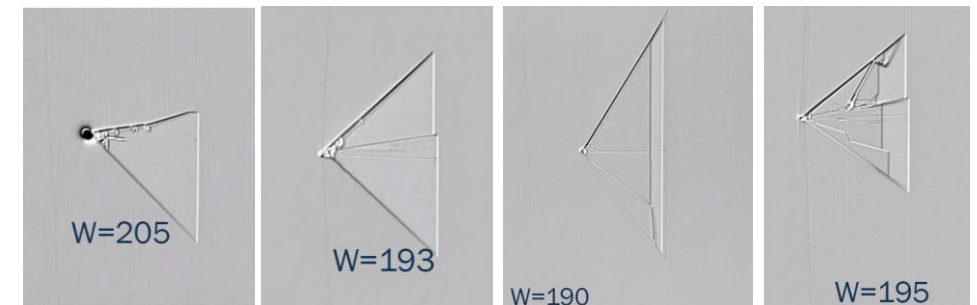
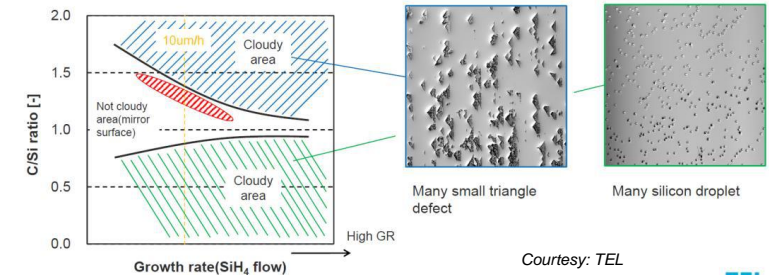
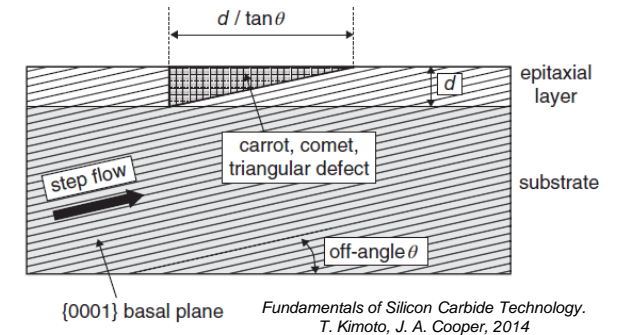
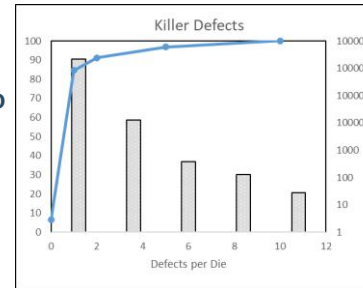
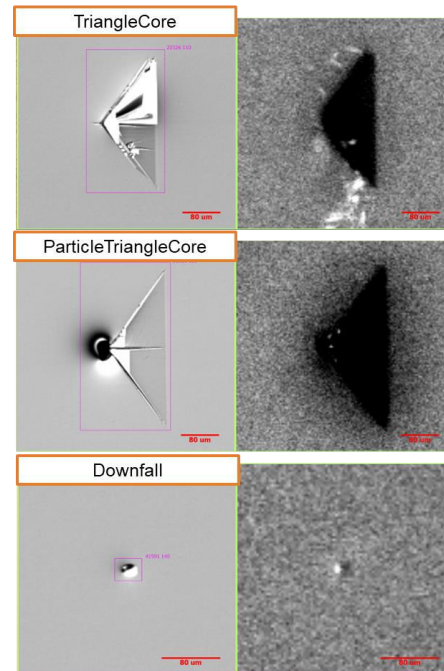


Fig. 4. (a) Normaski contrast of type A triangular defect and (b) the schematic showing its 3-dimensional configuration.

Jianqiu Guo et al: Understanding the microstructures of triangular defects in 4H-SiC homoepitaxial. Journal of Crystal Growth 480 (2017) 119–125







# SiC epitaxy technology for mass production

# SiC epitaxy reactors (Yole study 2023)

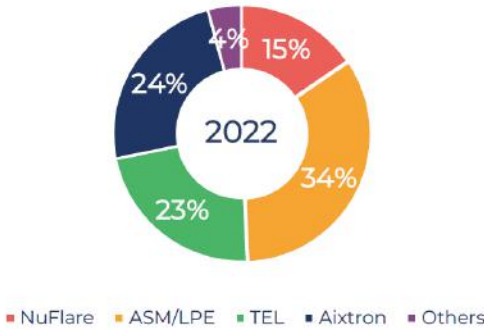
## SiC EPITAXY EQUIPMENT VENDORS

The change of landscape taking place in the past year.

The leading equipment vendors of SiC epitaxy include TEL, Aixtron, NuFlare, LPE(now part of ASM).



Market share by tools in units (Yole's estimation)



Power SiC 2023 | Report | [www.yolegroup.com](http://www.yolegroup.com) | 190

## Requirements for new generation SiC epitaxy reactors:

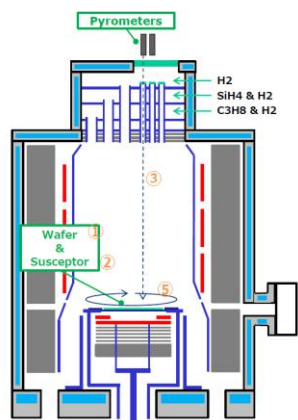
- Automated cassette-to-cassette systems.
- IT interface for Equipment integration.
- Clean room class 1-10; service area – grey room.
- Elevated loading/unloading temperature („idle“ temperature) = 600-900°C
- Metrics:
  - Throughput, uptime, footprint
  - Epi quality, stability
  - Cost per wafer
  - Customer and service support
  - Spare parts
  - Continuous improvement



# SiC epitaxy reactors

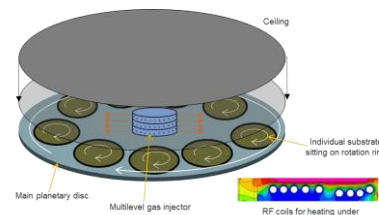
## NuFlare Epirevo S6/S8

- Vertical type single-wafer reactor
  - Complicated gas showerhead
  - Resistive heating
  - High rotation speed (up to 600 rpm)
  - Growth rate 50-60  $\mu\text{m/hr}$



## Aixtron G10

- Horizontal type batch reactor (planetary)
  - 9x150mm / 6x200mm configuration
  - Complicated planetary hardware
  - RF heating
  - Growth rate 20-30  $\mu\text{m/hr}$
  - High throughput



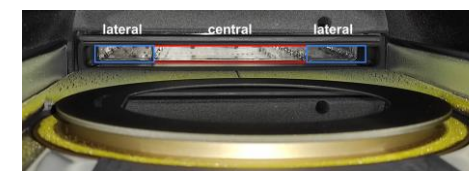
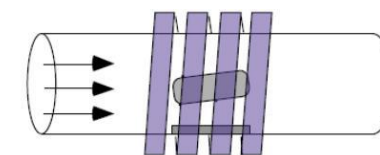
9x150 mm configuration



6x200 mm configuration

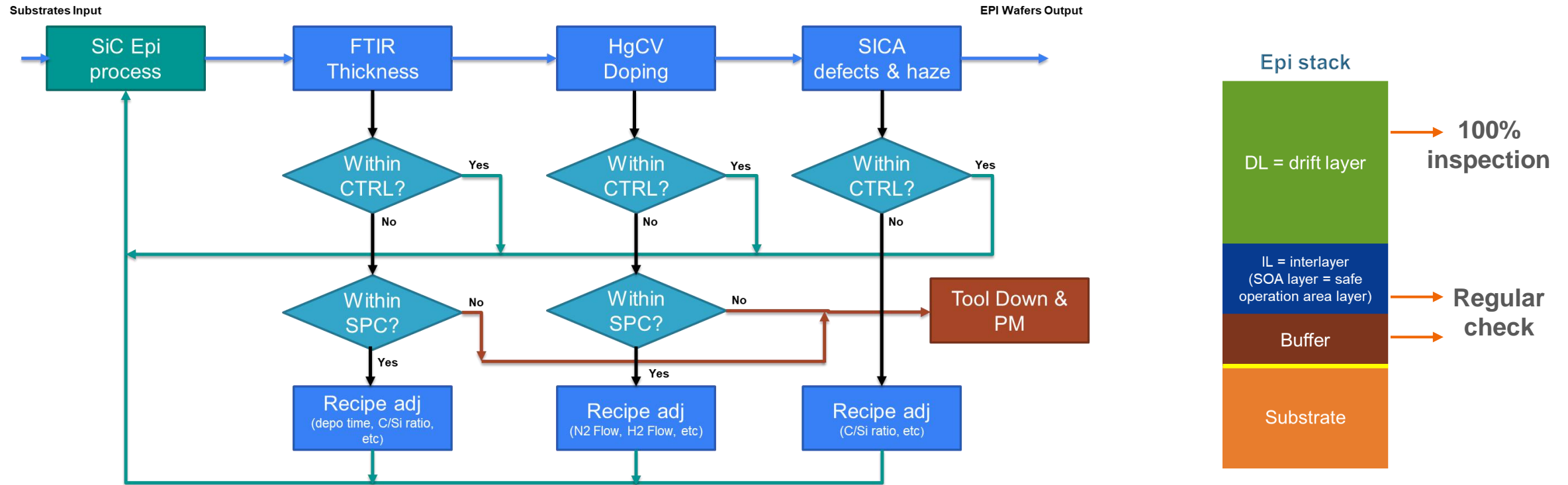
## LPE PE108 / PE208

- Horizontal type single-wafer reactor
  - Robust hardware design, RF heating
  - Growth rate 50-70  $\mu\text{m/hr}$
  - Excellent epi layer uniformity and process stability
  - Easy to switch between 150mm/200mm config





# Basic SiC Epitaxy Process Control Diagram



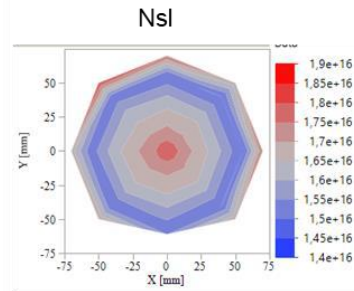
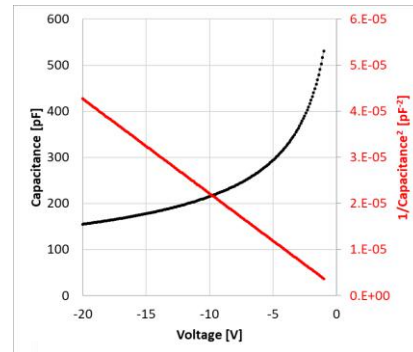
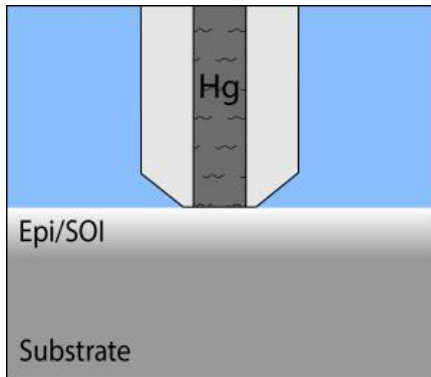
# Epi layer characterization

## Doping measurement

- Mercury C-V profiling
- Pneumatically controlled, non-damaging contact probe design
- Extremely stable contact area, highly repeatable CV measurement
- Capacitance-voltage profiling of Schottky barrier

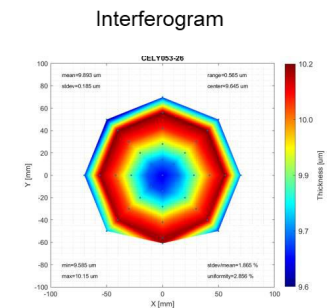
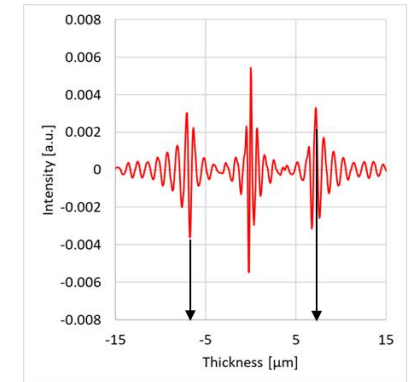
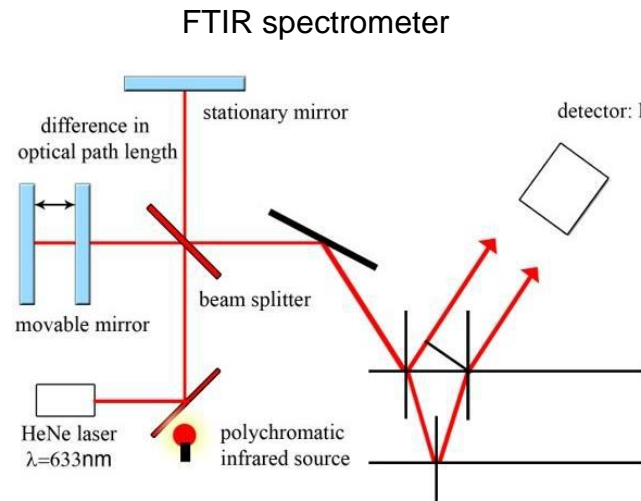
$$\frac{d}{dV_R} \left( \frac{1}{C^2} \right) = \frac{2}{A^2 e \epsilon \epsilon_0 \rho(W)}$$

$\rho(W)$  ... doping density at depth  $W$   
 $C$  ... capacitance  
 $V_R$  ... voltage  
 $A$  ... cross-sectional area  
 $e$  ... elementary charge  
 $\epsilon_0 = 8.8541878128 \cdot 10^{-14} \text{ F/cm}$   
 $\epsilon$  ... dielectric constant



## Thickness measurement

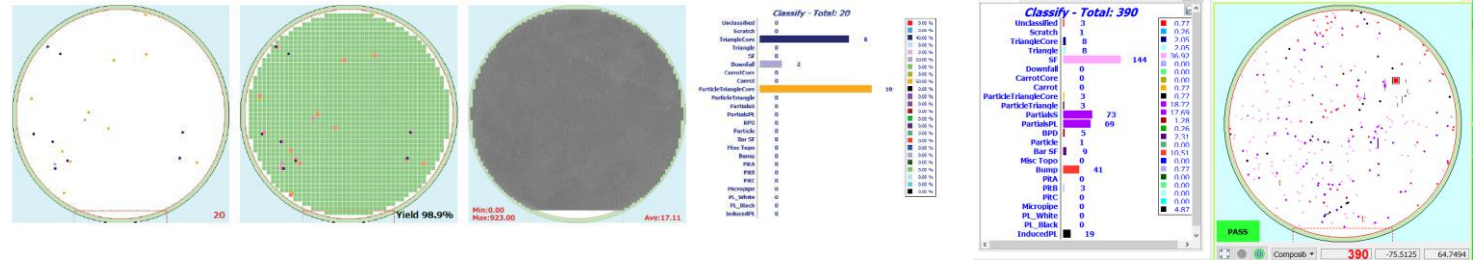
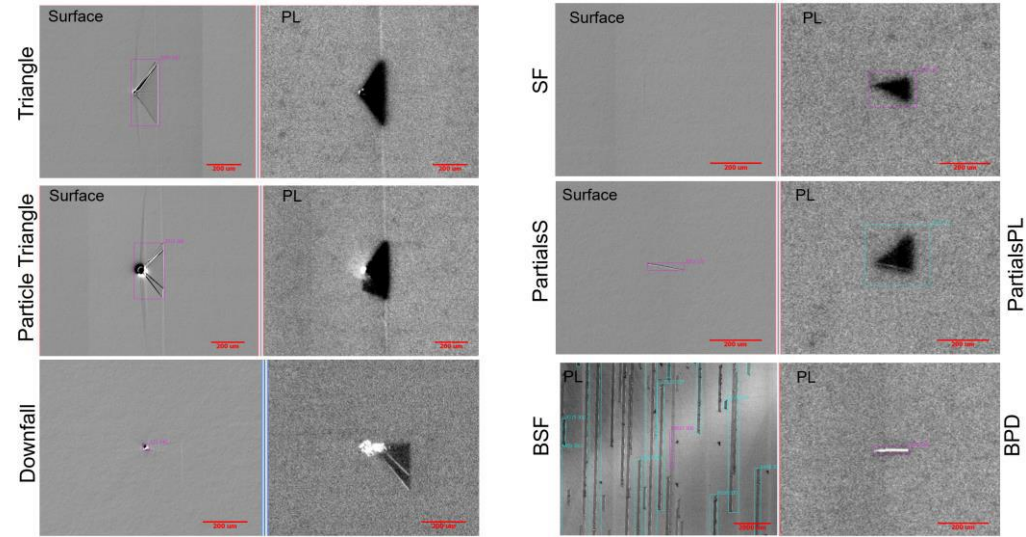
- Infra-Red Reflectometer (Michelson interferometer)
- EPI thickness directly calculated from the interferogram
- Side-bursts from constructive interference of the waves reflected from the top and the bottom surfaces of the EPI layer



# Surface epi defect measurement and classification



- Hg-Xe lamp for light source
- Multiple wavelength Band Pass filters on detection side for NUV and VIS PL
  - NIRW: 660nm-long pass
  - VIS: 400-525nm
  - NUV: 381-399nm
- ADC classification after training the dataset



- Chip yield prediction based on „killer defects“.
- Each classified defect has known position, size → every fabricated chip has known quantity and types of defects.





# Evolution & challenges in SiC epitaxy in recent years

# Dynamic evolution

Requirements for mass-production quality & control have evolved dramatically!

SiC Epi in 2021

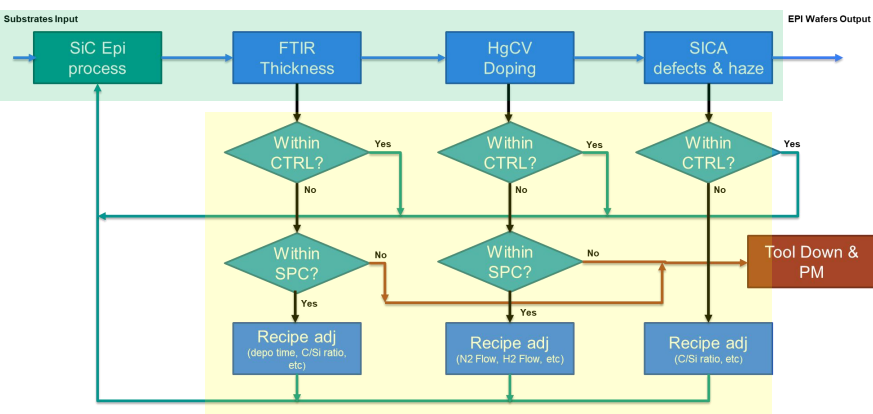


SiC Epi needed in 2025

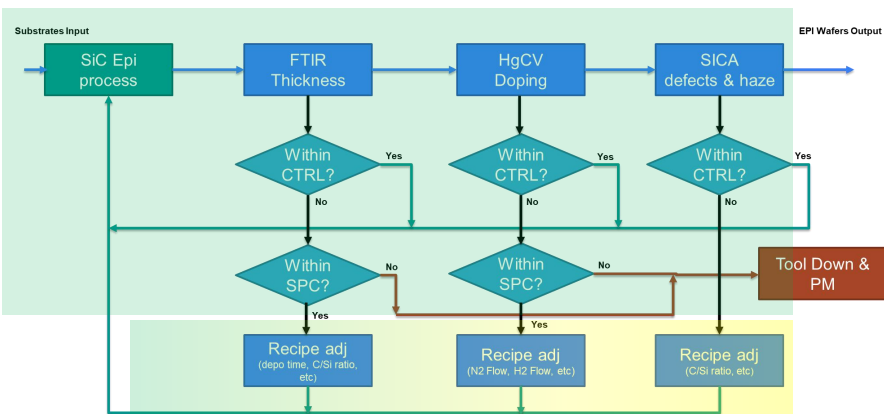


# Epi reactors and process control

- 2021: Equipment C2C, partially automated data collection
- Everything else done manually

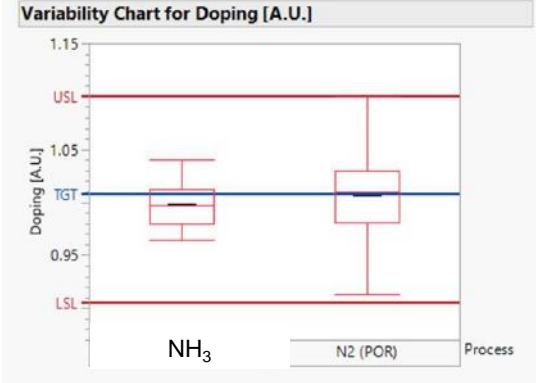


## 2024: on track to full automation



## Improved doping control: Change precursor to NH<sub>3</sub>

Molecule	Bond energy
Ethene	C=C: 610 kJ/mol
Propane	C-C: 348 kJ/mol
Silane	Si-H: 384 kJ/mol
HCl	H-Cl: 431 kJ/mol
TCS	382 kJ/mol
N <sub>2</sub>	956 kJ/mol
NH <sub>3</sub>	N-H: 388 kJ/mol



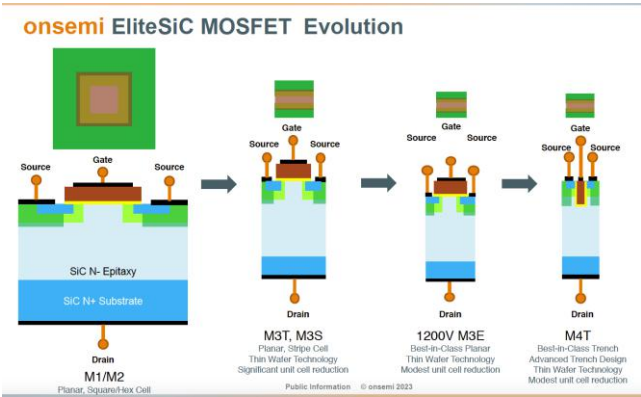
## Predictive maintenance: parts replacement for up-time & costs





# Thickness and doping requirements

- SiC MOSFET design evolution → huge challenge for epi



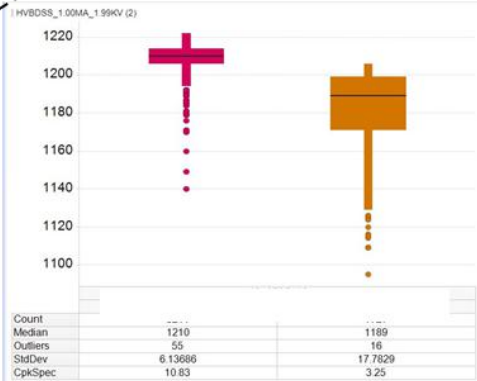
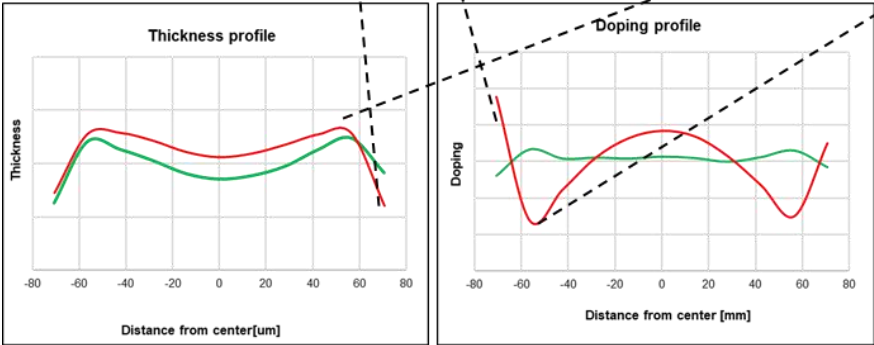
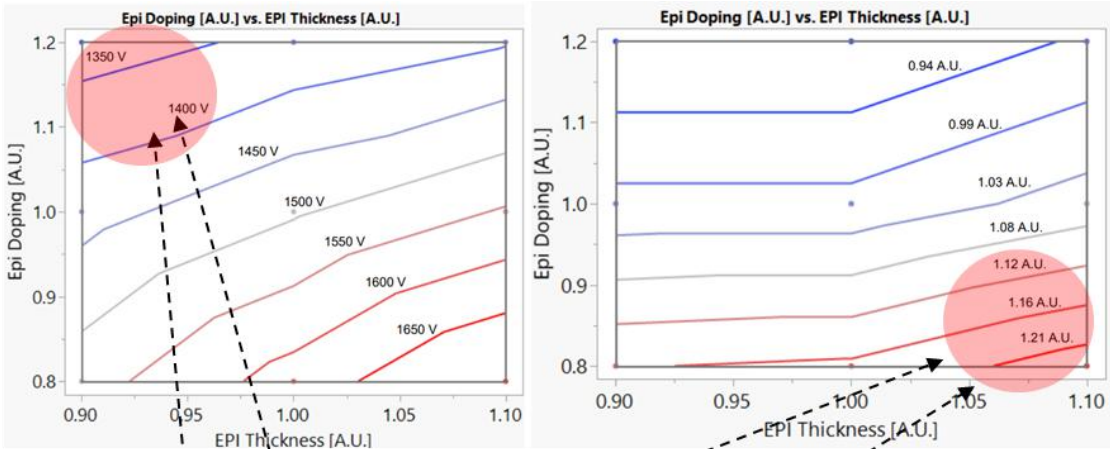
New generation epi:

- Thickness and doping profile matching
- Tighter spec for both, CPK to achieve 6σ process control
  - Within-wafer variability
  - Wafer-to-wafer

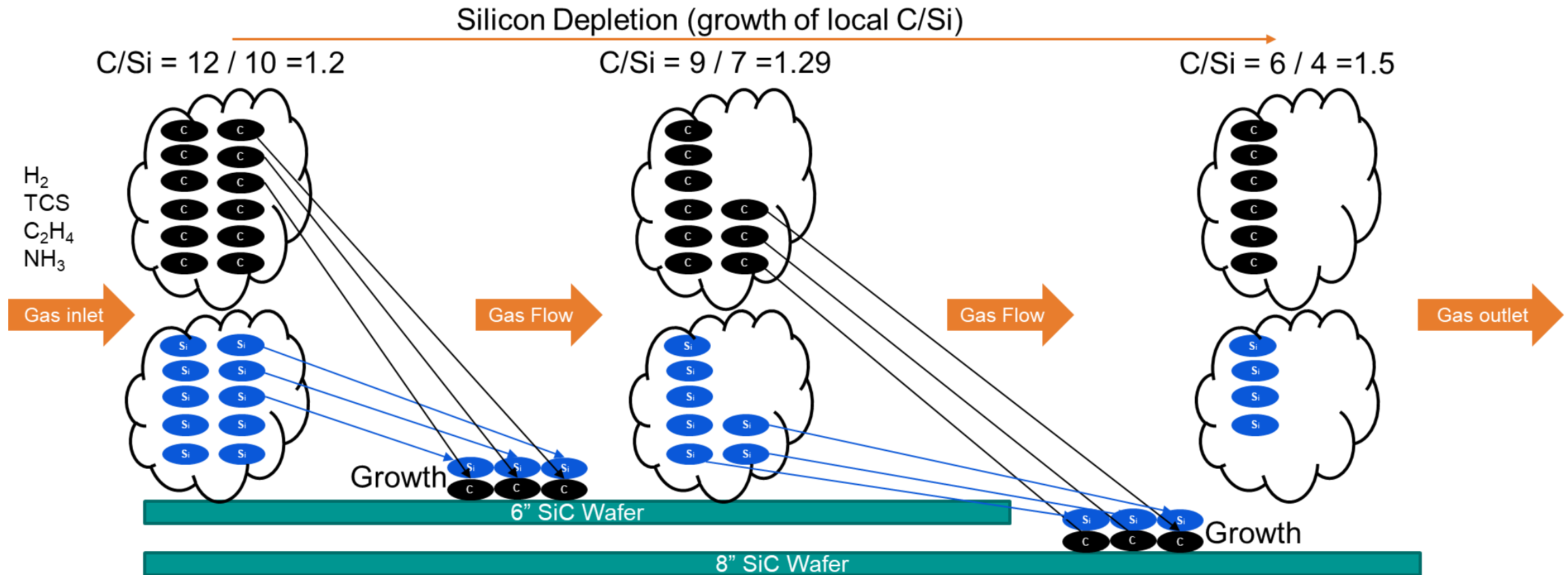
$$\frac{\sigma}{\text{mean}} < x\% \rightarrow \frac{\text{max}-\text{min}}{\text{max}+\text{min}} < x\%$$

Average on-wafer: Target +/- x%  
 → Allowed range (x) reduction by 33% or 50%

TCAD Simulation of BV<sub>dss</sub> and R<sub>sp</sub> as a Function of EPI Thickness and Doping



# 200mm epi process challenges



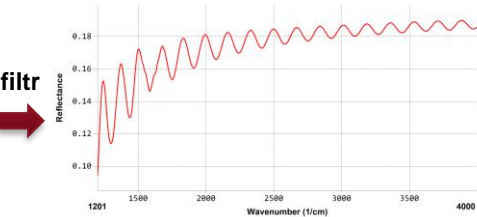
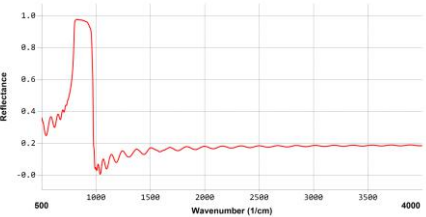
- Lower surface mobility of C compared to Si + requirement for good doping control (N substitutes C) requires  $C / Si > 1$ .
- $C / Si > 1$  leads to silicon depletion effect, effectively increasing  $C / Si$  along the deposition path →
  - 200 mm wafer are substantially more difficult for process control (thickness, doping, defects).

# Thickness measurement

- **Interferogram**: risk of incorrect side-burst identification
  - Interference from top buffer interface!
- Sensitive to buffer doping concentration
  - Interference from top buffer interface!
- Method is precise (repeatable, stable), but not accurate.
- It is not possible to distinguish individual epi layers

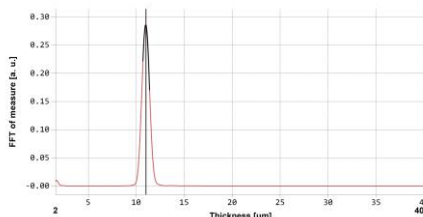


## Spectral reflectance

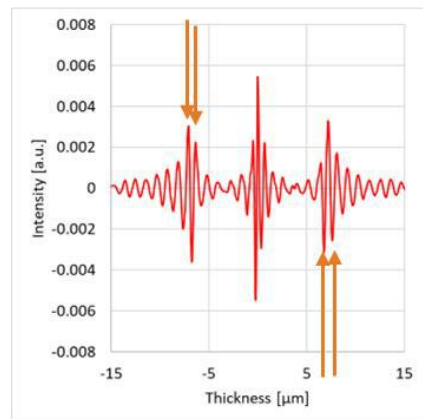


filt

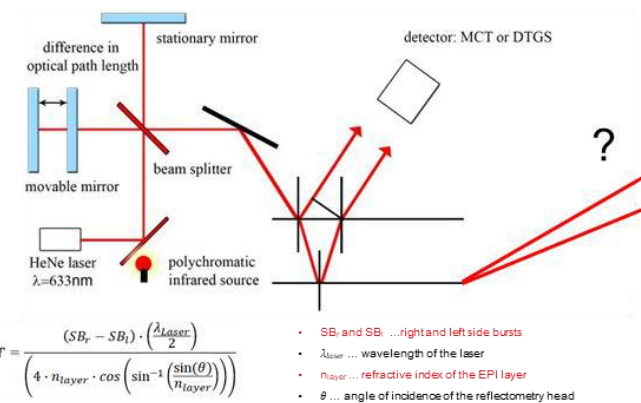
FFT



- Good agreement with reference methods
  - SIMS, X-SEM
  - Spectral reflectance modelling (external demos)
  - Optical measurements in MIR, FIR

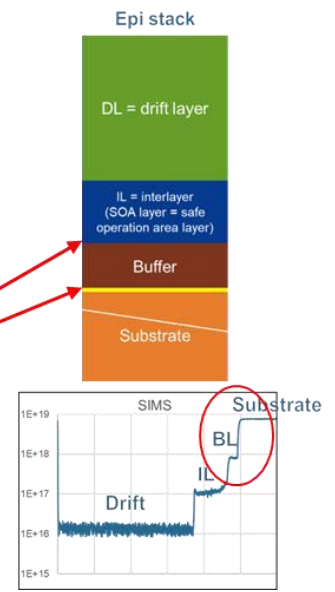


## POR method: Subtracted Interferogram



$$T = \frac{(SB_r - SB_l) \cdot \left(\frac{\lambda_{laser}}{2}\right)}{\left(4 \cdot n_{layer} \cdot \cos\left(\sin^{-1}\left(\frac{\sin(\theta)}{n_{layer}}\right)\right)\right)}$$

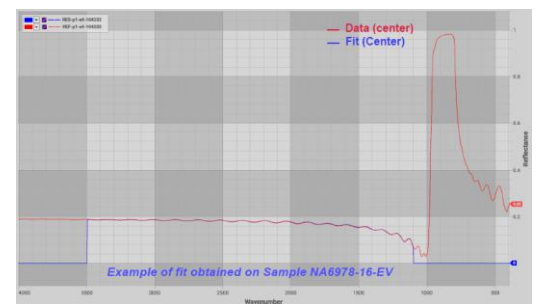
- $SB_r$  and  $SB_l$  ... right and left side bursts
- $\lambda_{laser}$  ... wavelength of the laser
- $n_{layer}$  ... refractive index of the EPI layer
- $\theta$  ... angle of incidence of the reflectometry head



## Can we measure individual layers?

- Reflectance spectrum (IR) modelling → **individual layer information**
- Usually Layers 2+3 are not distinguishable (doping dependent)
- Additional info: **substrate and buffer carrier concentration**

L3	Layer 3	Constant Model
L2	Layer 2	Drude Model (Free C. C.)
L1	Layer 1	Drude Model (Free C. C.)
	Substrate	Drude Model (Free C. C.)

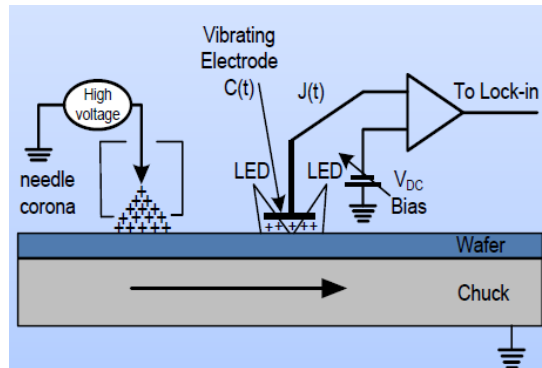




# Doping measurement

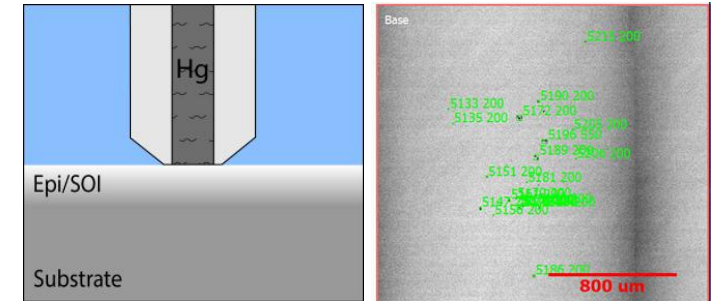
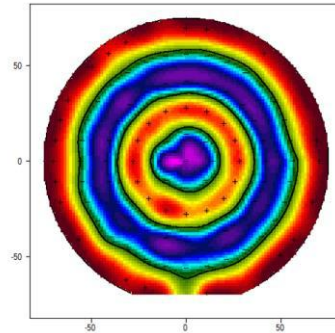
- HgCV is contact method → risk of surface contamination and damage
- Alternative: CnCV (Corona-charge Noncontact C-V)
  - Enables also defect evaluation by QUAD mapping

corona charging + Kelvin probe  $\Rightarrow$  Non-contact C-V  
 $\Delta Q_C$   $V = V_0 + \Delta V$   $C = \frac{\Delta Q_C}{\Delta V}$  vs.  $V$

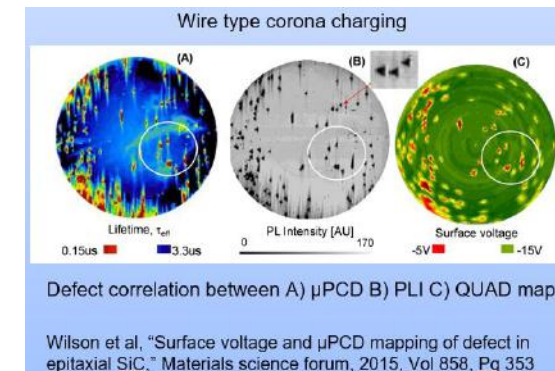


Vibrating Kelvin probe and corona discharge apparatus used in the measurements of dopant concentration, dielectric charge, interface state density and HEMT properties.

Courtesy: Semilab



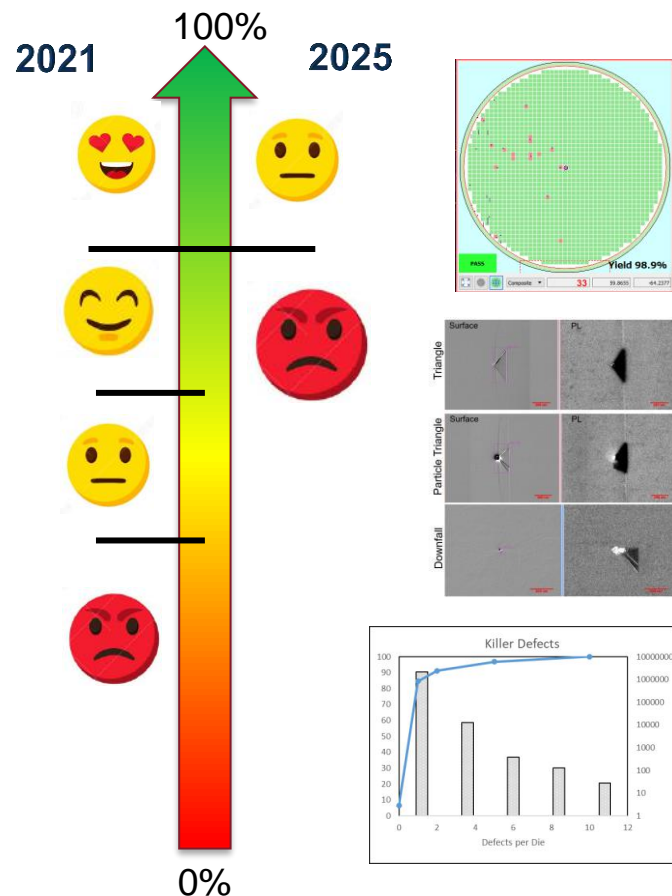
- CnCV QUAD mapping: defects in depletion region
- Surface voltage is mapped after Corona charge is applied and with time delay
- Large  $\Delta V \rightarrow$  Defects
  - Deep level emission increasing ionized defect concentration in the depletion region.
  - Defect related leakage current neutralizing the corona surface ions.



Courtesy: Semilab

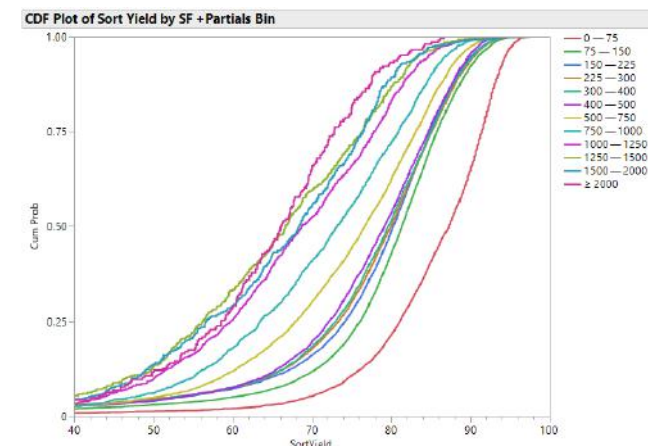
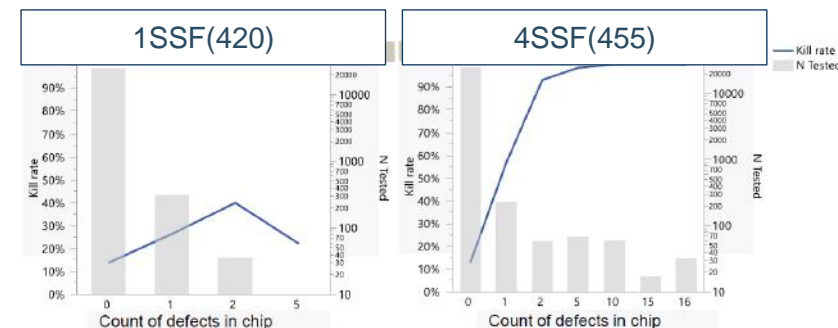
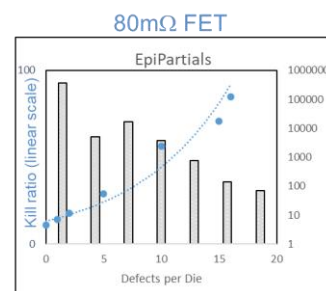
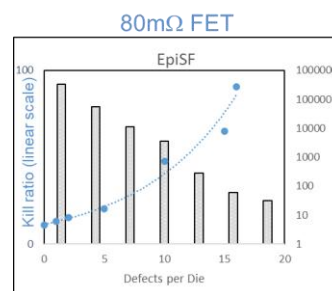
# Defects control and classification

Killer defect yield (% of good die prediction, not in scale)

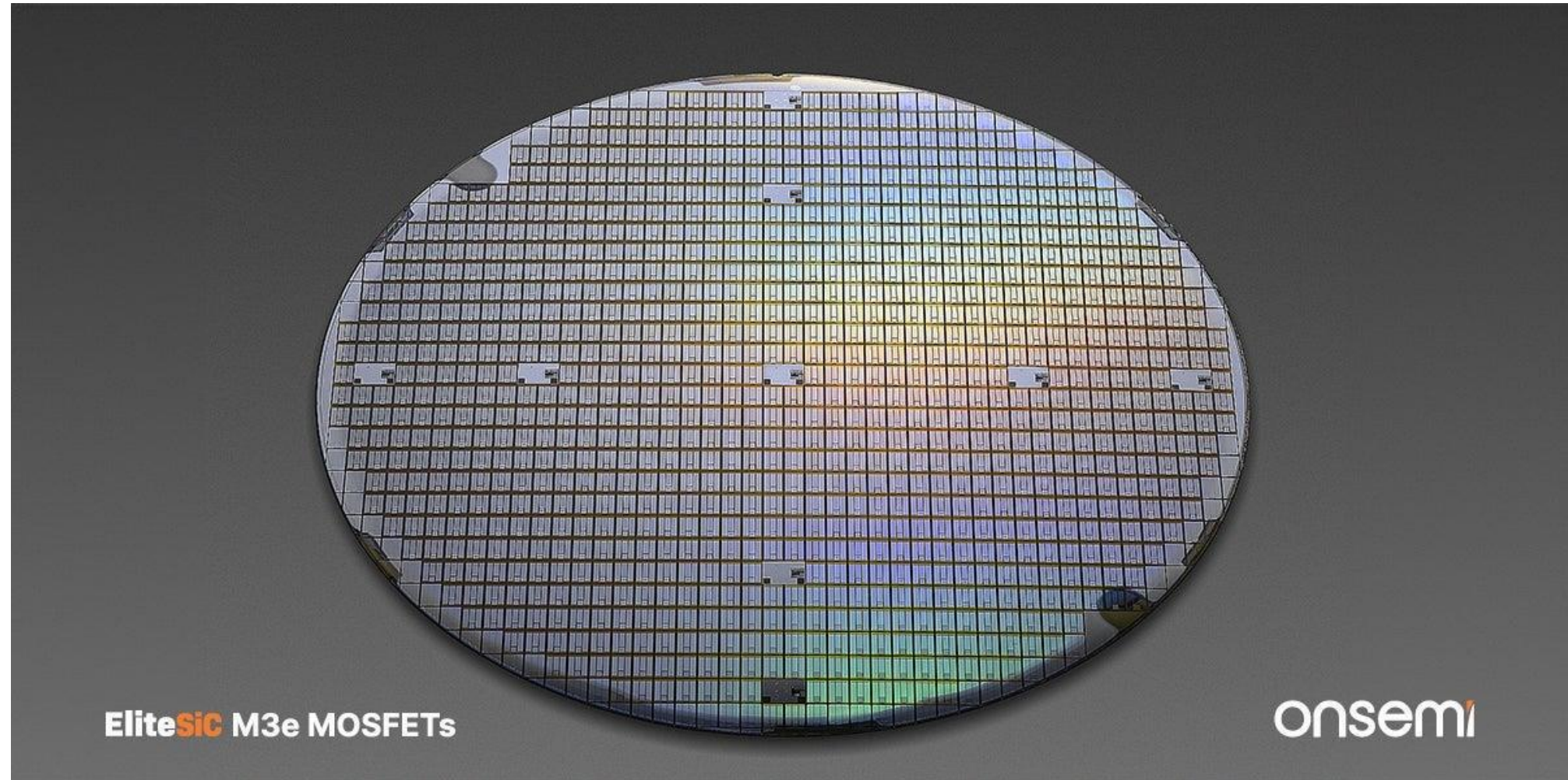


- With improved „killer“ defect yield, the effect of „non-killer“ defects becomes also critical
- High density of some defects (Stacking Faults, Partials) results in device parametric shifts, wide distribution, eventually out-of-spec parameters
- Leakage current degradation →  $BV_{dss}$  or  $V_{TH}$  issues,
- BSF: high quantity can affect  $R_{DS(on)}$
- Large data set are needed to correlate individual epi defects with device performance and set new specs
- Subclassification of different Stacking Faults, Partials, Triangles etc

$$KillRate = \frac{Failed\ chips}{All\ tested\ chips}$$



# Q&A







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